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10/598,552	06/13/2007	Johannus Theodorus Matheus Dielissen	NL040218	7218

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EXAMINER	
MOHEBBI, KOUROUSH	

ART UNIT	PAPER NUMBER
2471	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,552	DIELISSEN, JOHANNUS THEODORUS MATHEUS	
	Examiner	Art Unit	
	KOUROUSH MOHEBBI	2471	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/05/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is response to application number 10598552 and applicant amendment and argument dated on 07/22/2009.

Response to Arguments

2. Applicant's arguments filed 07/22/2009 have been fully considered but they are not persuasive.

Applicant argues in pages 6 that " the instructions of Endecott are not comparable to the packets claimed". Endecott instructions constructed as 8-bit wide (word) and 4 words deep (32 bits per instruction), the applicant of the current application describes the packet in specification page 7, lines 32-33 as "the packets are each 8-bit wide and 3 words deep. However, other bit widths and word depths are also possible".

Applicant argues in pages 6 that "matching said not required bits of said at least one inspected packet with other bits of the same packet. Rather the Endecott packet would replace the unused bits (not required bits) in one packet by bits of another packet (i.e., instructions) in a manner similar to that shown in Figure 2A". Endecott discloses method with aim of reducing the average Hamming distance between successive values by assigning values to unused bits (page 1, 4th paragraph, page 2, 4th paragraph).

Applicant amendment to claims 1 and 5 as described in page 7, recited " the element that unused bits are in a header related to a path over an interconnection". The added elements, even supported by specification and

narrowing down the claims, they consider as design choice and do not add substantial value to be considered as invention. The described advantages in specification, optimization and minimizing the power consumption (page 8, lines 14-16) and low implementation cost (page 9, lines 5-12) are met by assigning values to unused bits from bits of words of the same packet or bits of another packet with the aim of minimizing hamming distance between successive values (page 1, 4th paragraph, page 2, 4th paragraph).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 5 are rejected under 35 U.S.C. 102 (b) as being anticipated by Endecott et al. (WO. 02/095574).

Claim 1, Endecott discloses Integrated circuit (Fig. 1 in SoC, System on a Chip) having a plurality of processing modules (M, S) (Microprocessor, Fig. 1, el. 2 and memory (storage processing module), el. 4; page 2, 3rd paragraph) and an interconnect means (N) (buses, Fig. 1, el. 6; page 2, 3rd paragraph) for coupling said plurality of processing modules (M, S) (Microprocessor, Fig. 1, el. 2 and

memory (storage processing module), el. 4; page 2, 3rd paragraph) and for enabling a packet based communication (program instruction fetch; page 2, 7th paragraph) based on transactions (instructions are communicated between processor and memory; page 2, 7th paragraph) between said plurality of processing modules (M, S) (Microprocessor, Fig. 1, el. 2 and memory (storage processing module), el. 4), wherein each packet (instruction) comprises a first predetermined number of subsequent words (instructions as shown in page 3 consist of 32 bits and 4 words of 8 bits. Page 7 shows input/output instructions as eight bits long for sake of simplicity of the explanation; page 3, 2nd paragraph) each having a second predetermined number of bits (8 bits long words (byte) are illustrated in page 5-7), wherein a first of said plurality of processing modules (M) (Microprocessor) issues a transaction (fetch) by sending at least one packet (fetching instruction) over said interconnect means (bus) to a second of said plurality of processing modules (S) (storage processing module) (page 2, 6th and 7th paragraphs), comprising:

at least one packet inspecting unit (PIU) for inspecting bits (Endecott discloses assigning values to unused bits of instructions in order to reduce Hamming distance between successive data values (page 9 , 2nd paragraph; abstract, page 1), Endecott's method necessarily includes instruction inspection unit (a module, which includes software and hardware, the software resides in memory Fig. 1, el. 4 and executed by microprocessor Fig. 1, el. 2) to detect instruction's unused bits in order to assign values to the unused bits and reduce

Hamming distance) with of said at least one packet to determine bits not required (unused bits, page 3, 1st and 6th paragraphs; see also pages 5 and 6, unused bits marked as X) for said issued transaction and for matching said not required bits (unused bits) in said header of said at least one inspected packet related to a path over said interconnect with other header bits related to said path of the same packet (reducing hamming distance between successive values; page 1, 4th paragraph, page 2, 4th paragraph; copying /matching bits from preceding or following instruction of words of instructions into instruction's unused bits and minimizing the Hamming distance is described in page 6; see also page 8, 4th paragraph).

Claim 2, Endecott further discloses wherein said at least one packet inspecting unit (PIU) is adapted to match said not required bits with previous or following bits in the same packet (Endecott in page 8, 4th paragraph describes the process of matching unused bits with either preceding or following bits of the instruction, the Endecott's method necessarily includes one inspecting module to detect the unused bits of instructions and match them to optimize Hamming distance).

Claim 3, Endecott further discloses wherein said at least one packet inspecting unit (PIU) (Endecott's method necessarily includes instruction inspection unit (a module, which includes software and hardware, the software

resides in memory Fig. 1, el. 4 and executed by microprocessor Fig. 1, el. 2) to detect instruction's unused bits in order to assign values to the unused bits and reduce Hamming distance) is further adapted to match said not required bits with corresponding bits in a previous or following word in the same packet (Endecott describes 32 bit long instruction size according to the format of page 3, 2nd paragraph, in pages 5 and 6, Endecott describes smaller size (8 bits) instruction for sake of simplification of the discussion and in page 8, 4th paragraph describes one bit at the time matching to achieve Hamming distance optimization. Endecott describes a method to reduce average Hamming distance between successive values (general term), which can reduce Hamming distance between words in one instruction or between instructions and by no means limited to instruction fetch, see page 2, 6th and 4th paragraphs).

Claim 5, Endecott discloses method for packet switching control in an integrated circuit (Fig. 1 in SoC, System on a Chip) having a plurality of processing modules (M, S) (Microprocessor, Fig. 1, el. 2 and memory (storage processing module), el. 4; page 2, 3rd paragraph) and an interconnect means (N) (buses, Fig. 1, el. 6; page 2, 3rd paragraph) for coupling said plurality of processing modules (M, S) and for enabling a packet based communication (program instruction fetch; page 2, 7th paragraph) based on transactions (instructions are communicated between processor and memory (storage processing module); page 2, 7th paragraph) between said plurality of processing

modules (M, S) (Microprocessor, Fig. 1, el. 2 and memory (storage processing module), el. 4; page 2, 3rd paragraph), wherein each packet (instruction) comprises a first predetermined number of subsequent words (instructions as shown in page 3 consist of 32 bits and 4 words of 8 bits. Page 7 shows input/output instructions as eight bits long for sake of simplicity of the explanation; page 3, 2nd paragraph) each having a second predetermined number of bits (8 bits long words (byte) are illustrated in page 5-7), wherein a first of said plurality of processing modules (M) (Microprocessor) issues a transaction (fetch) by sending at least one packet (fetching instruction) over said interconnect means (bus) to a second of said plurality of processing modules (S) (storage processing module) (page 2, 6th and 7th paragraphs) , comprising the steps of:

inspecting bits of said at least one packet (instruction) to determine bits not required (unused bits, page 3, 1st and 6th paragraphs; see also pages 5 and 6, unused bits marked as X) for the issued transaction and updating said not required bits (unused bits) of said at least one inspected packet with other bits of the same packet , wherein said unused bits are related to a path over said interconnection (reducing hamming distance between successive values; page 1, 4th paragraph, page 2, 4th paragraph; copying /matching bits from preceding or following instruction or words of instructions into instruction's unused bits and minimizing the Hamming distance is described in page 6; see also page 8, 4th paragraph).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endecott et al. (WO. 02/095574) in view of Ricciulli, et al. (US 2004/0202190).

Claim 4, Endecott discloses all the limitation of claim 2.

Endecott does not disclose comprising:

at least one network interface (NI) associated to said first of said plurality of processing modules (I) for controlling the communication between said first of said plurality of processing modules (I) and said interconnect means (N), wherein each of said at least one packet inspecting units (PIU) is arranged in one of said network interfaces (NI).

Ricciulli discloses at least one network interface (NI) (Network Interface card; ¶0036) associated to said first of said plurality of processing modules (I) (Fig. 2, el. 103; ¶ 0009) for controlling the communication between said first of said plurality of processing modules (I) (Fig. 2, el. 103; ¶ 0009) and said interconnect means (N) (Fig. 2, el. 210; ¶0030), wherein each of said at least one

packet inspecting units (PIU) (high speed packet inspecting; Fig. 2, el. 201; ¶0036; ¶0031; ¶0038) is arranged in one of said network interfaces (NI) (Network Interface card; ¶0036).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to add packet inspecting unit (PIU) to network interface interconnect one internal-coupling port to one external-coupling port as taught by Ricciulli to modify Endecott system to inspect data stream against predetermined network rules and apply signature matching. The motivation would be inspecting (header fields, payload, CRC bits) of data packet stream base on specified rules (packet signature) for further processing and modification of the packets, which would make the system enable to implement Endecott teaching of determining Hamming distance and matching unused bits of the packets in a single processing module or in larger server system (¶0009; ¶0038).

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The reference Hurd Linda L. (US Patent 6,535,984 B1) discloses of optimizing assembly code of multiple instruction words to reduce power usage of processor.
The reference Takano et al. (US Patent 5,790,874 B1) discloses an instruction sequence optimization apparatus to reduce processor power consumption by minimizing Hamming distance between consecutive instructions.

The reference Takayama (US Patent 6,725,450 B1) discloses a program conversion apparatus, the converted machine language instructions have less digit bit changes.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KOUROUSH MOHEBBI whose telephone number is (571)270-7908. The examiner can normally be reached on Monday to Thursday, 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. M./
Examiner, Art Unit 2416

/Chi H Pham/
Supervisory Patent Examiner, Art Unit 2471